Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of generating an ASIC design database using each piece of software of a simulation tool, a logic synthesis tool, a timing analysis tool, a logic simulation tool, and a power consumption calculation tool, comprising:

~~extracting~~ executing, when a function design using description data comprising a header portion and an entity portion has been performed, ~~information necessary for reuse design from various execution results of the entity portion;~~ simulation by the simulation tool;

generating a simulation result list of the simulation;

extracting a simulation time from the simulation result list;

writing the extracted simulation time ~~information necessary for reuse design~~ in the header portion of the description data;

inputting the entity portion of the description data to the logic synthesis tool and executing a logic synthesis;

outputting a gate-level net list;

inputting the net list to the timing analysis tool and executing a timing analysis;

outputting an analysis report as an analysis result;

comparing values in the analysis report with pre-input desirable specifications;

extracting, if the compared values satisfy the desirable specifications, timing information and layout area information, and writing the timing and layout area information in the header portion of the description data;

executing a logic simulation for the gate-level net list by the logic simulation tool;

inputting simulation data to the power consumption calculation tool and carrying out a power consumption calculation process;

outputting a power consumption calculation result list;

extracting power consumption information from the power consumption calculation result list and writing the power consumption information in the header portion of the description data; and

storing, as one file at a predetermined location, the description data comprising the header portion in which the information necessary for reuse is written, and the entity portion.

2. (Original) A method of generating an ASIC design database, according to claim 1, wherein the information necessary for reuse, which is extracted from the various execution results of the entity portion, is at least a simulation time, layout area, timing and power consumption.

3. (Original) A method of generating an ASIC design database, according to claim 1, wherein the entity portion of said description data is described using a hardware description language.

4. (Original) A method of generating an ASIC design database, according to claim 1, wherein the entity portion of said description data is RTL description data described in a register transfer level.

5. (Currently amended) A method of generating an ASIC design database, according to claim ~~1~~ 4, wherein the file stored at the predetermined location, information written in the header portion and RTL description data in the entity portion are uniformly managed.

6. (Currently amended) A method of generating an ASIC design database using each piece of software of a simulation tool, a logic synthesis tool, a timing analysis tool, a logic simulation tool, and a power consumption calculation tool, comprising:

~~extracting~~ executing, when a function design using RTL description data comprising a header portion and an entity portion ~~and made in a register level~~ has been performed, ~~information necessary for reuse design from various execution results of the entity portion~~ simulation by the simulation tool;

generating a simulation result list of the simulation;

extracting a simulation time from the simulation result list;

writing the extracted ~~information necessary for reuse design~~ simulation time in the header portion of the RTL description data;

inputting the entity portion of the description data to the logic synthesis tool and executing a logic synthesis;

outputting a gate-level net list;

inputting the net list to the timing analysis tool and executing a timing analysis;

outputting an analysis report as an analysis result;

comparing values in the analysis report with pre-input desirable specifications;

extracting, if the compared values satisfy the desirable specifications, timing information and layout area information, and writing the timing and layout area information in the header portion of the RTL description data;

executing a logic simulation for the gate-level net list by the logic simulation tool;

inputting simulation data to the power consumption calculation tool and carrying out a power consumption calculation process;

outputting a power consumption calculation result list;

extracting power consumption information from the power consumption calculation result list and writing the power consumption information in the header portion of the RTL description data; and

storing, as one file at a predetermined location, the RTL description data comprising the header portion in which the information necessary for reuse is written, and the entity portion.

7. (Withdrawn) A method of generating an ASIC design database, comprising:

performing, when a function design has been carried out by an RTL description composed of a header portion and an entity portion and made in a register transfer level, a simulation using a simulation tool with respect to the entity portion of the RTL description;

extracting a simulation time from a simulation result and writing the simulation time in the header portion of the RTL description;

inputting the entity portion of the RTL description to a logic synthesis tool and logic-synthesizing the entity portion, and outputting a gate-level net list;

inputting the output gate-level net list to a timing analysis tool, and outputting a timing analysis result report;

comparing values of the timing analysis result report with preset conditions;

extracting a timing value and a layout area information, which are the result of the analysis result report with preset conditions;

extracting a timing value and a layout area information, which are the result of the analysis, when said conditions are met, and writing the extracted timing value and layout area information in the header portion of the RTL description;

performing a logic simulation using a logic simulation tool with respect to the gate-level net list;

inputting data of the logic simulation to a power consumption calculation tool, and outputting a power consumption calculation result;

extracting a power consumption from the power consumption calculation result, and writing the power consumption in the header portion of the RTL description; and

storing, as one file at a predetermined location, the TRL description comprising the header portion in which the simulation time, and timing value, the layout area information and the power consumption are written, and the entity portion.